

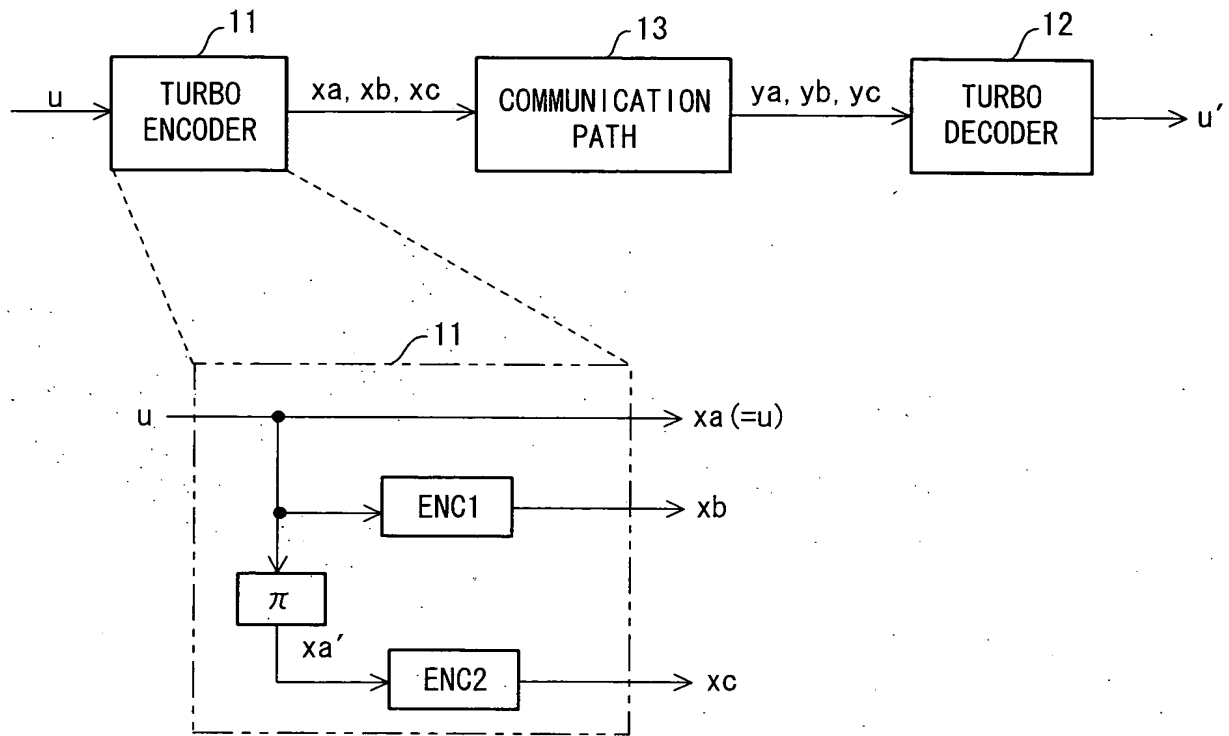
FIG. 1

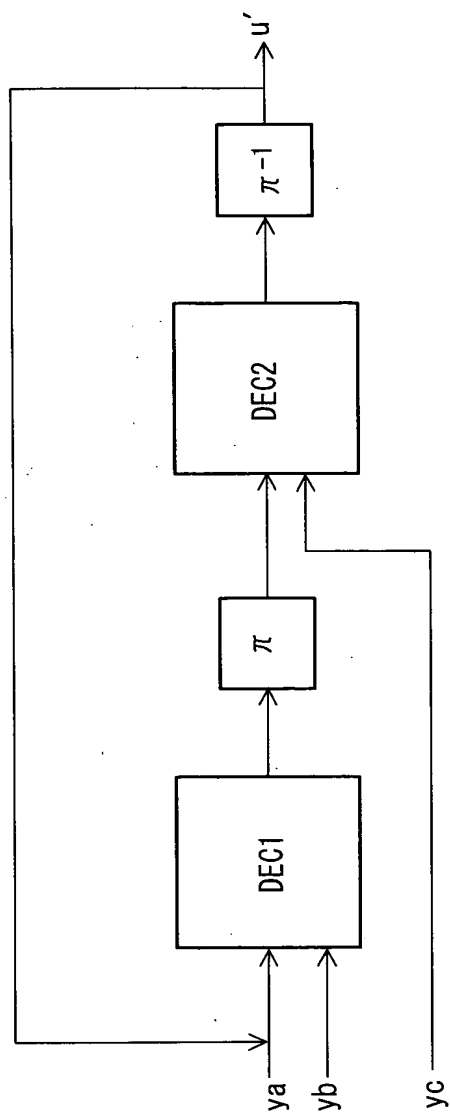
FIG. 2

FIG. 3

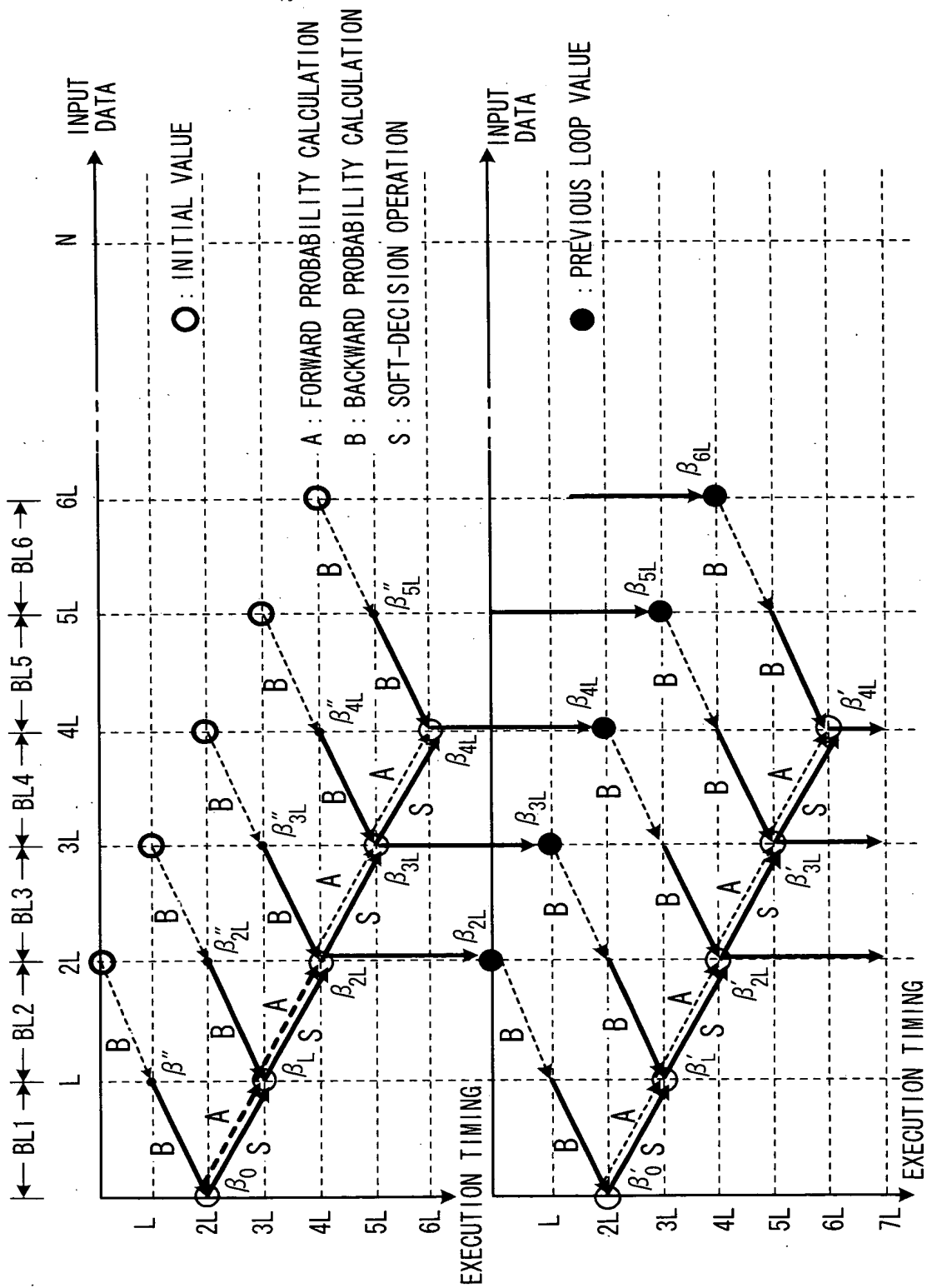


FIG. 4

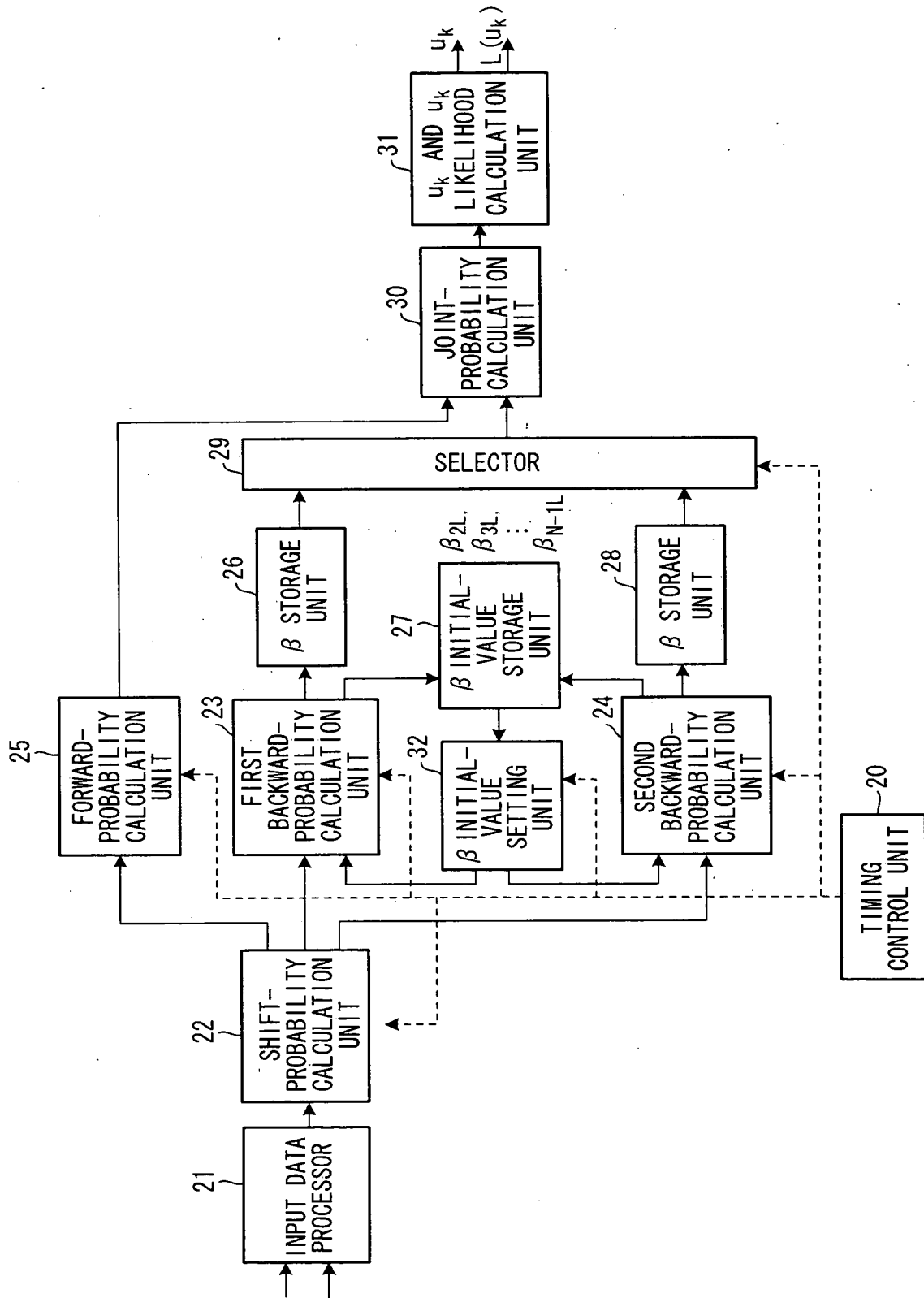


FIG. 5

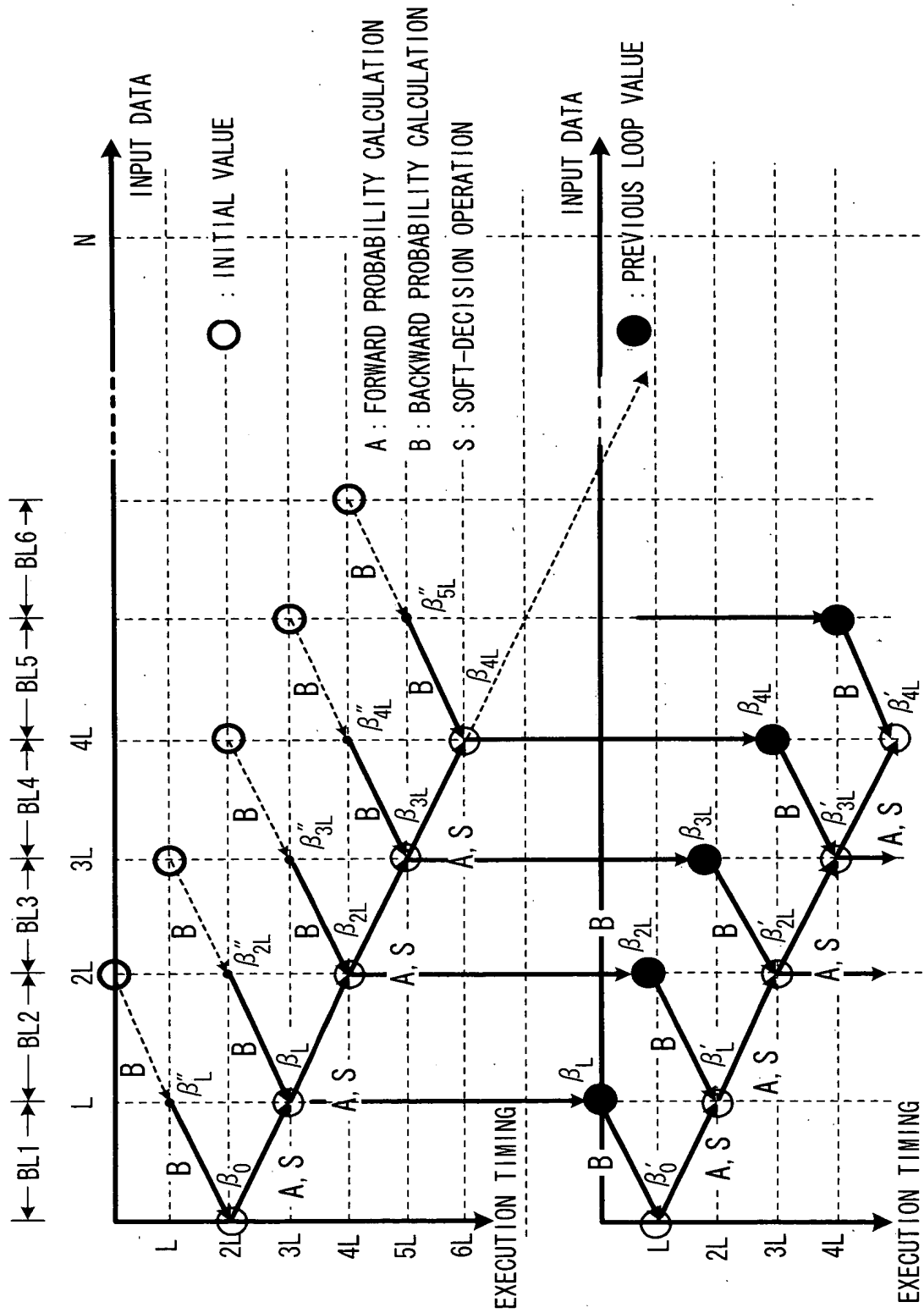


FIG. 6

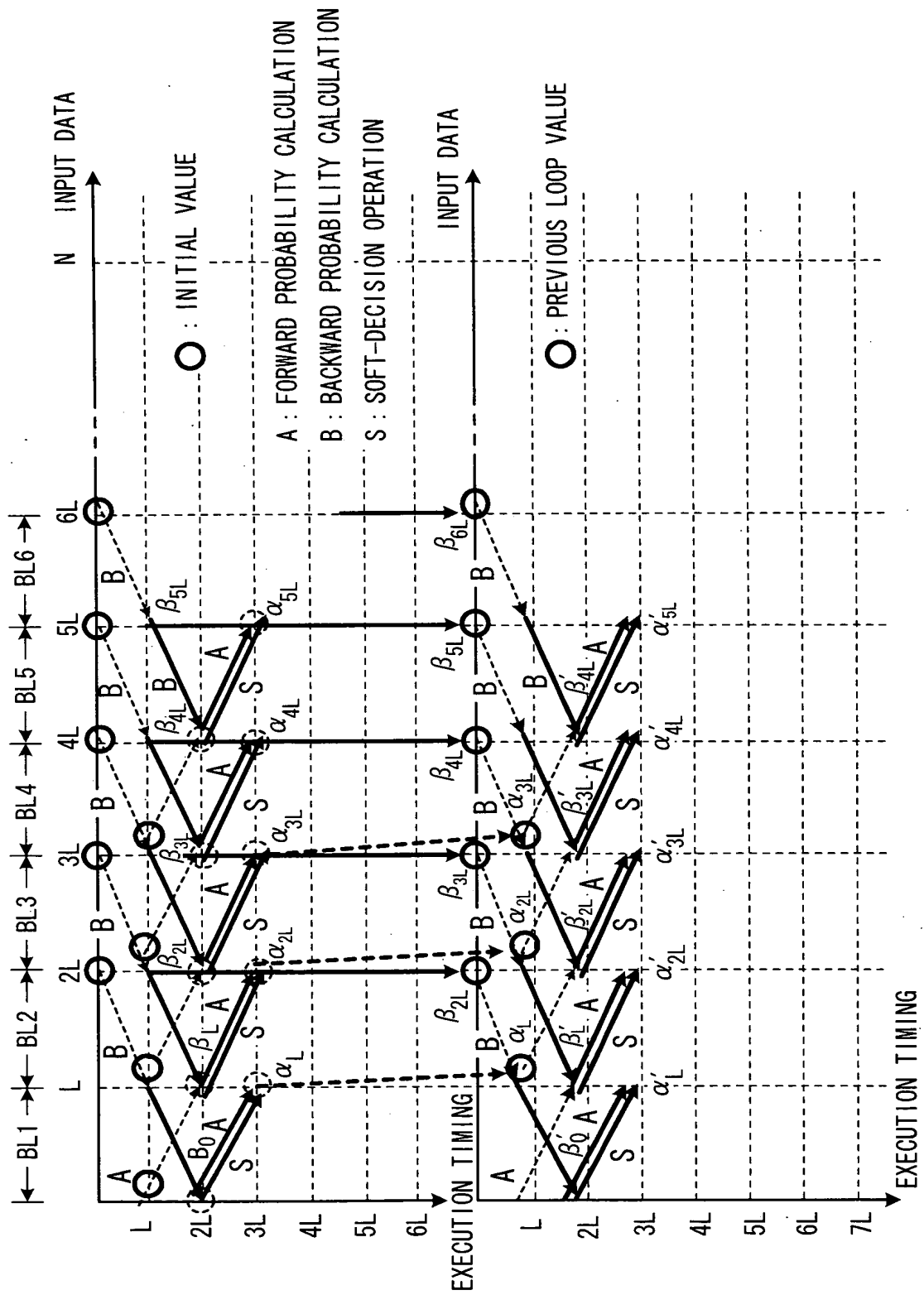


FIG. 7

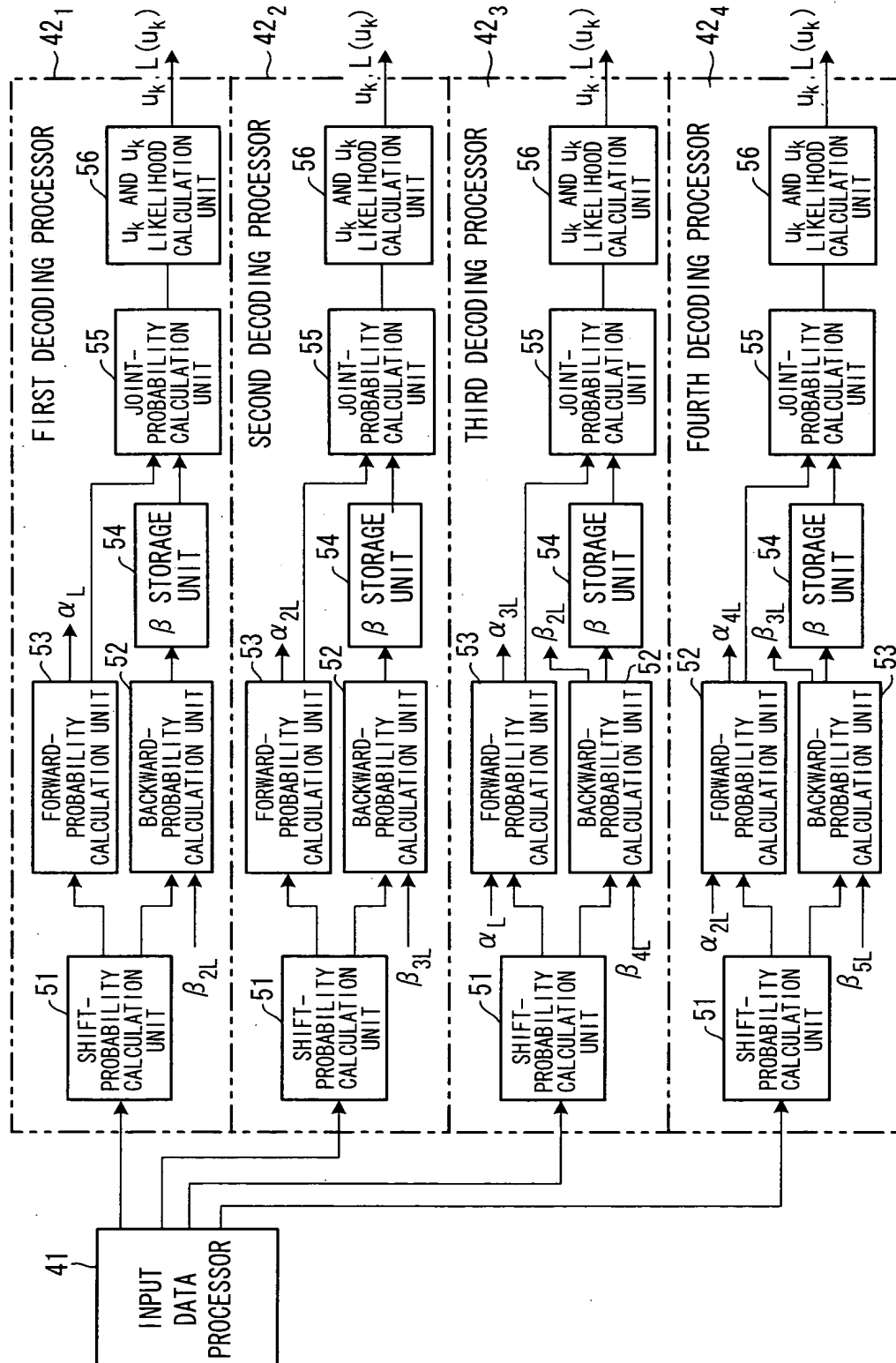


FIG. 8

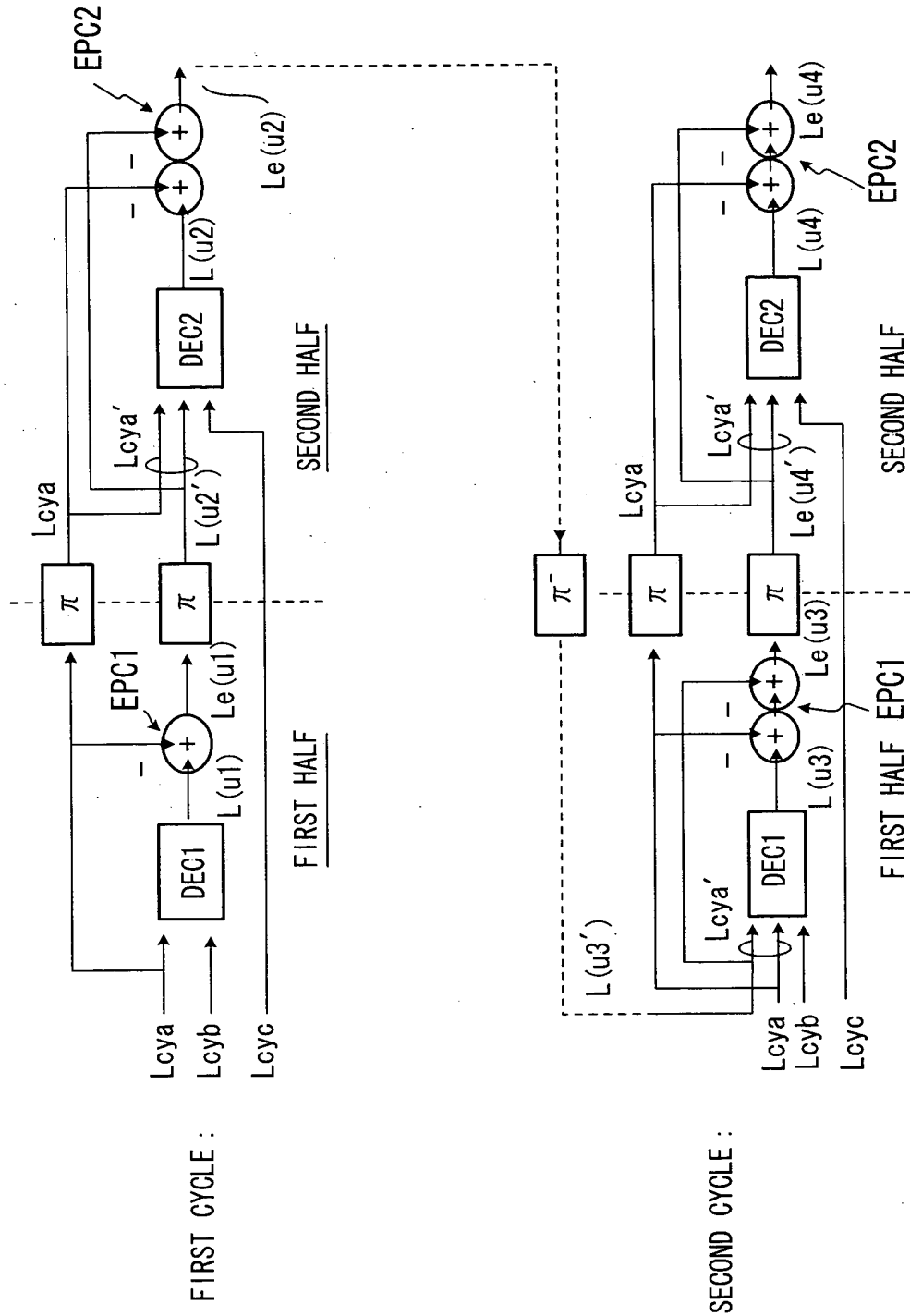
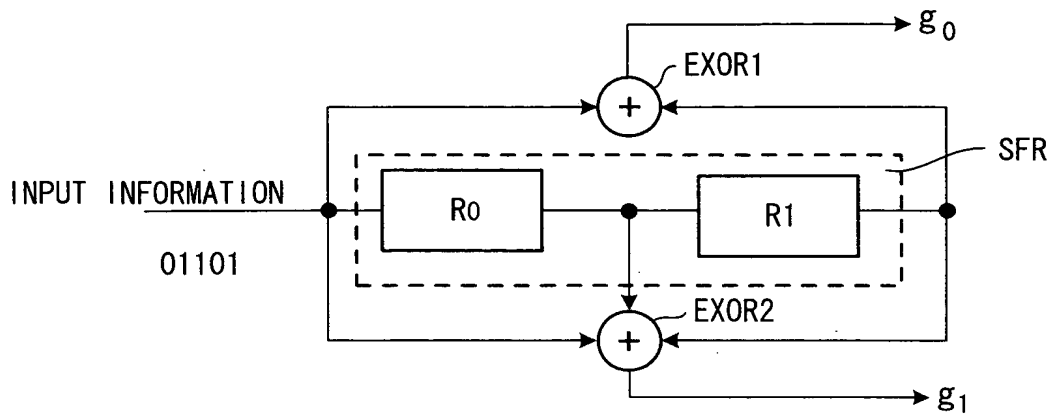


FIG. 9 PRIOR ART**FIG. 10 PRIOR ART**

INPUT	INITIAL STATE	SHIFT REGISTER		OUTPUT	
		0	0	g_0	g_1
0	→	0	0	0	0
1	→	1	0	1	0
1	→	1	1	0	1
0	→	0	1	1	1
1	→	1	0	1	0
		state			

FIG. 11 PRIOR ART

m_0	m_1	m_2	m_3
0 0	0 1	1 0	1 1

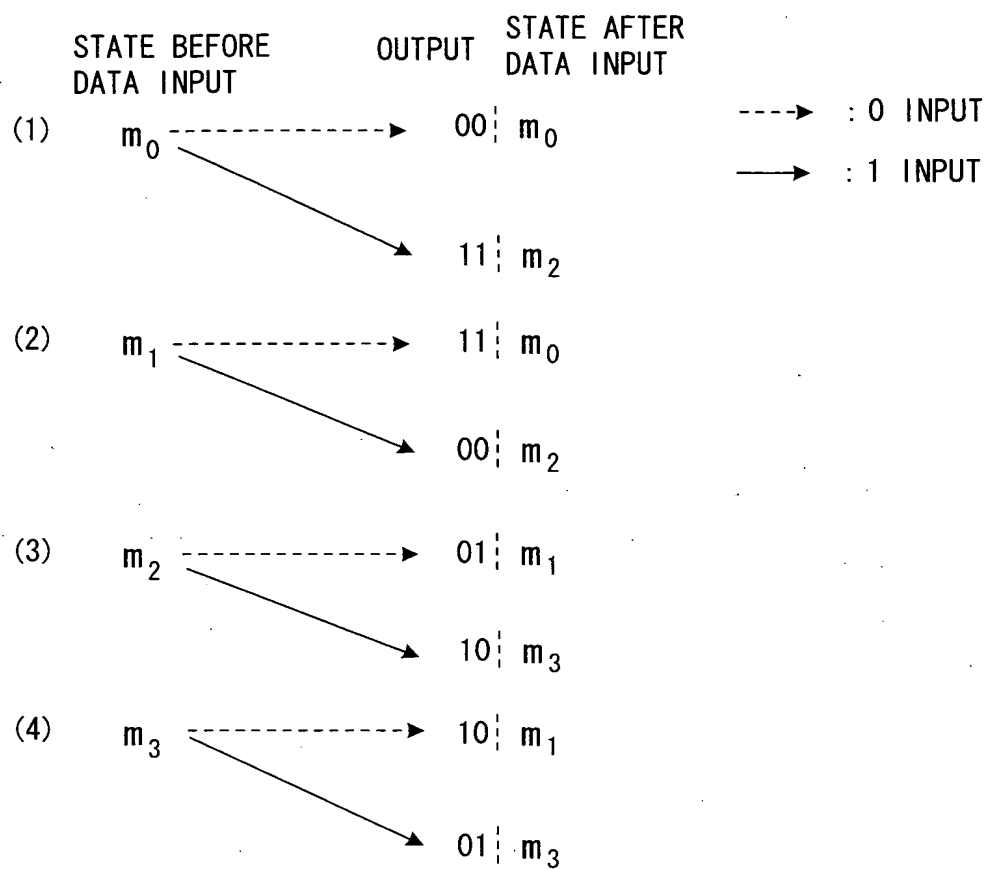
FIG. 12 PRIOR ART

FIG. 13 PRIOR ART

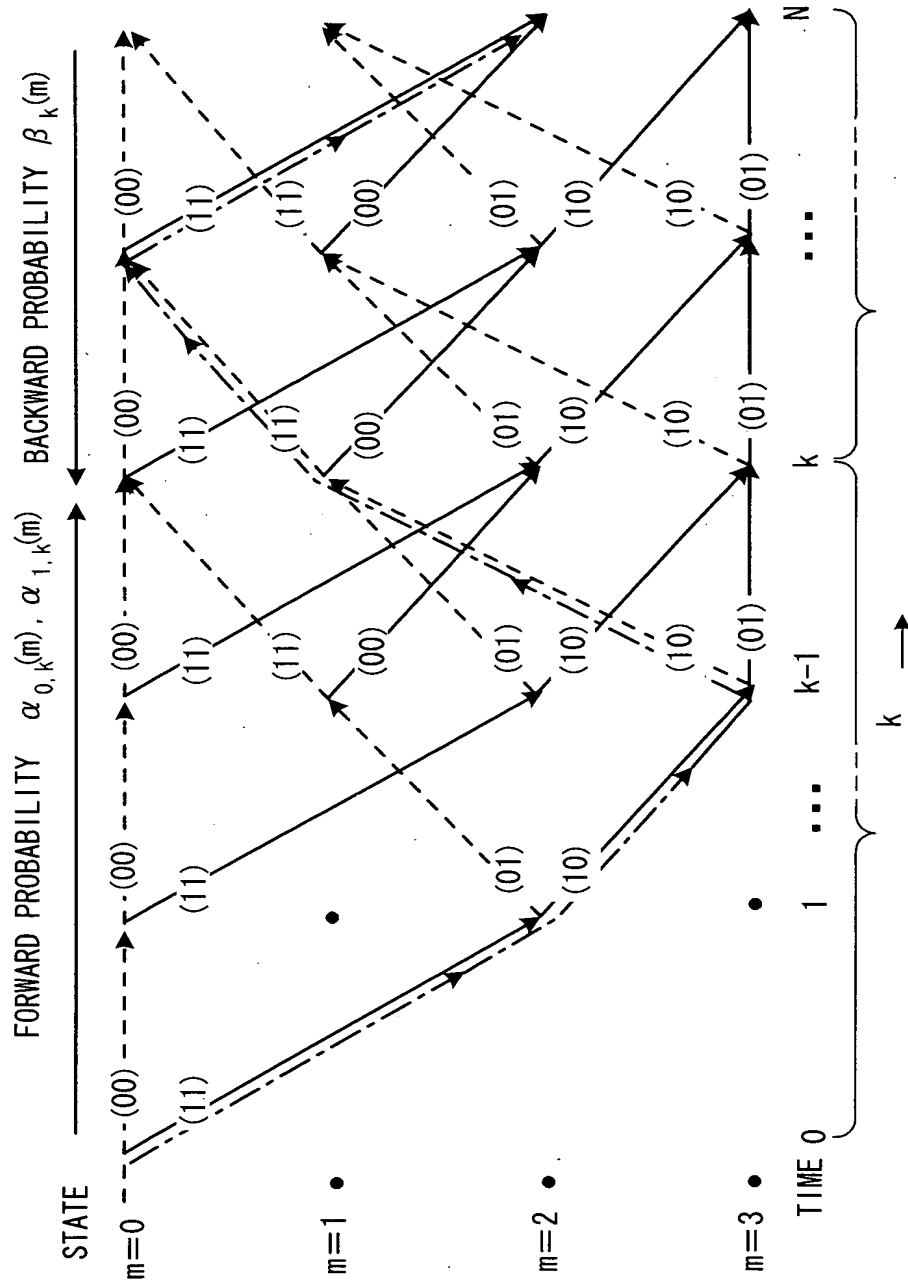


FIG. 14 PRIOR ART

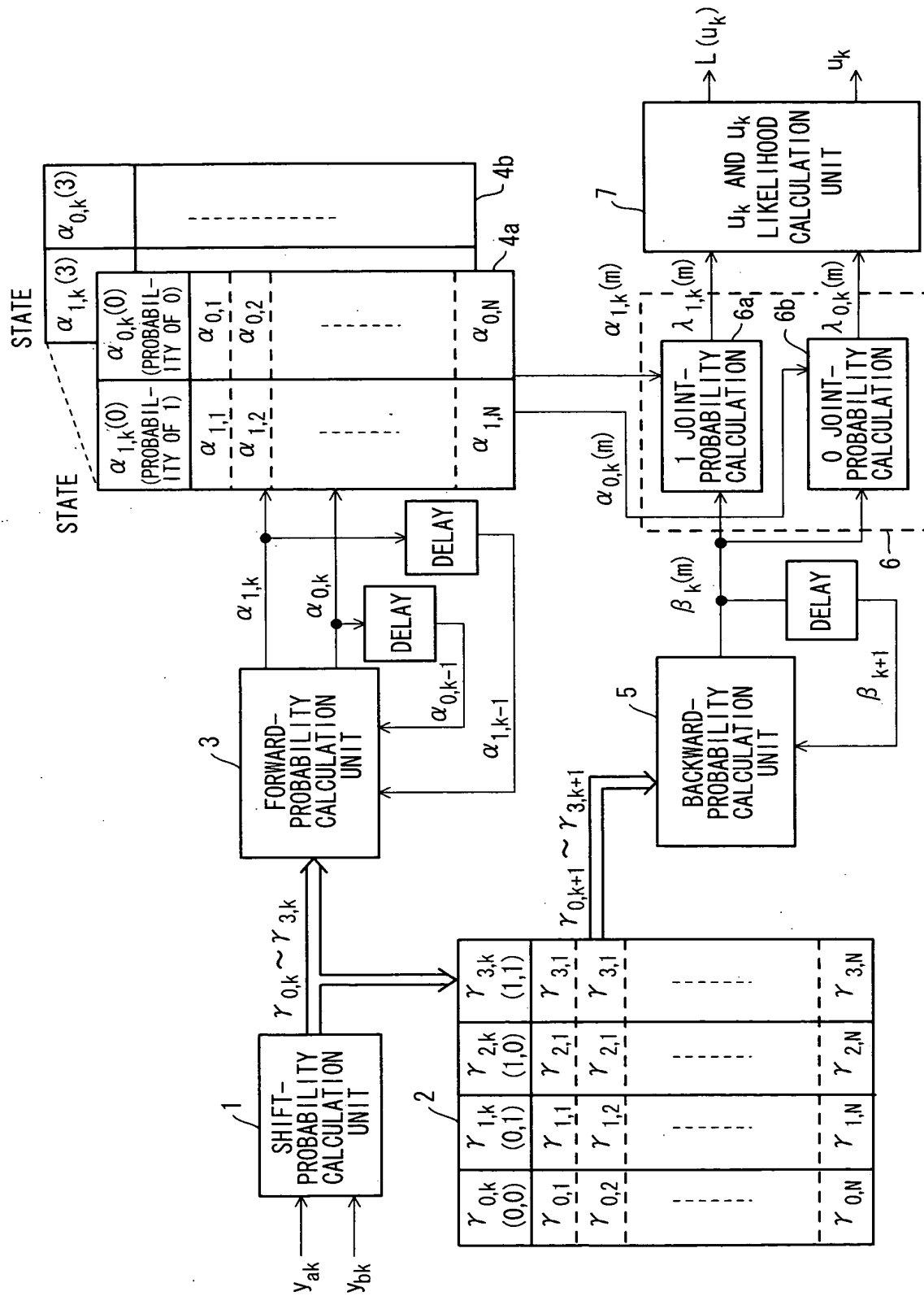


FIG. 15 PRIOR ART

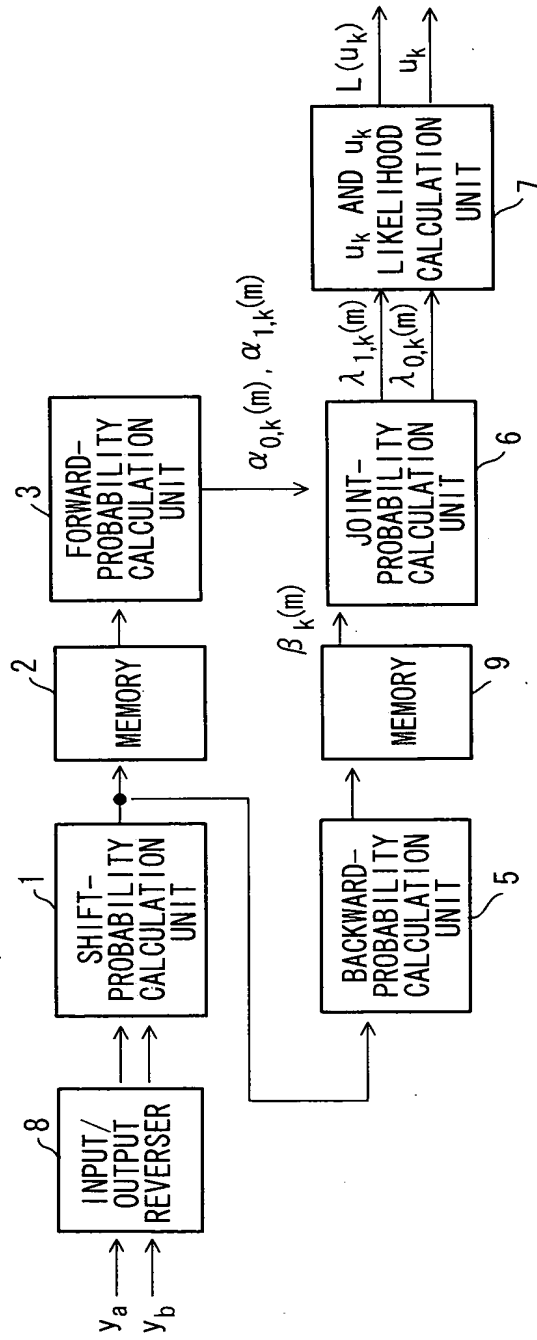


FIG. 16 PRIOR ART

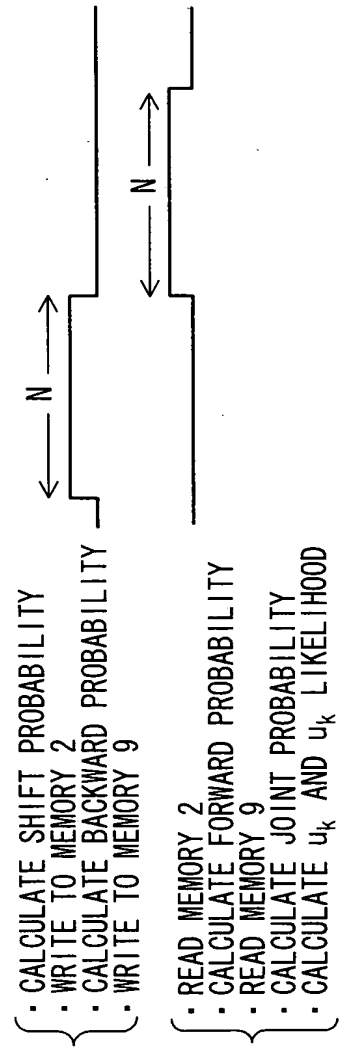


FIG. 17 PRIOR ART

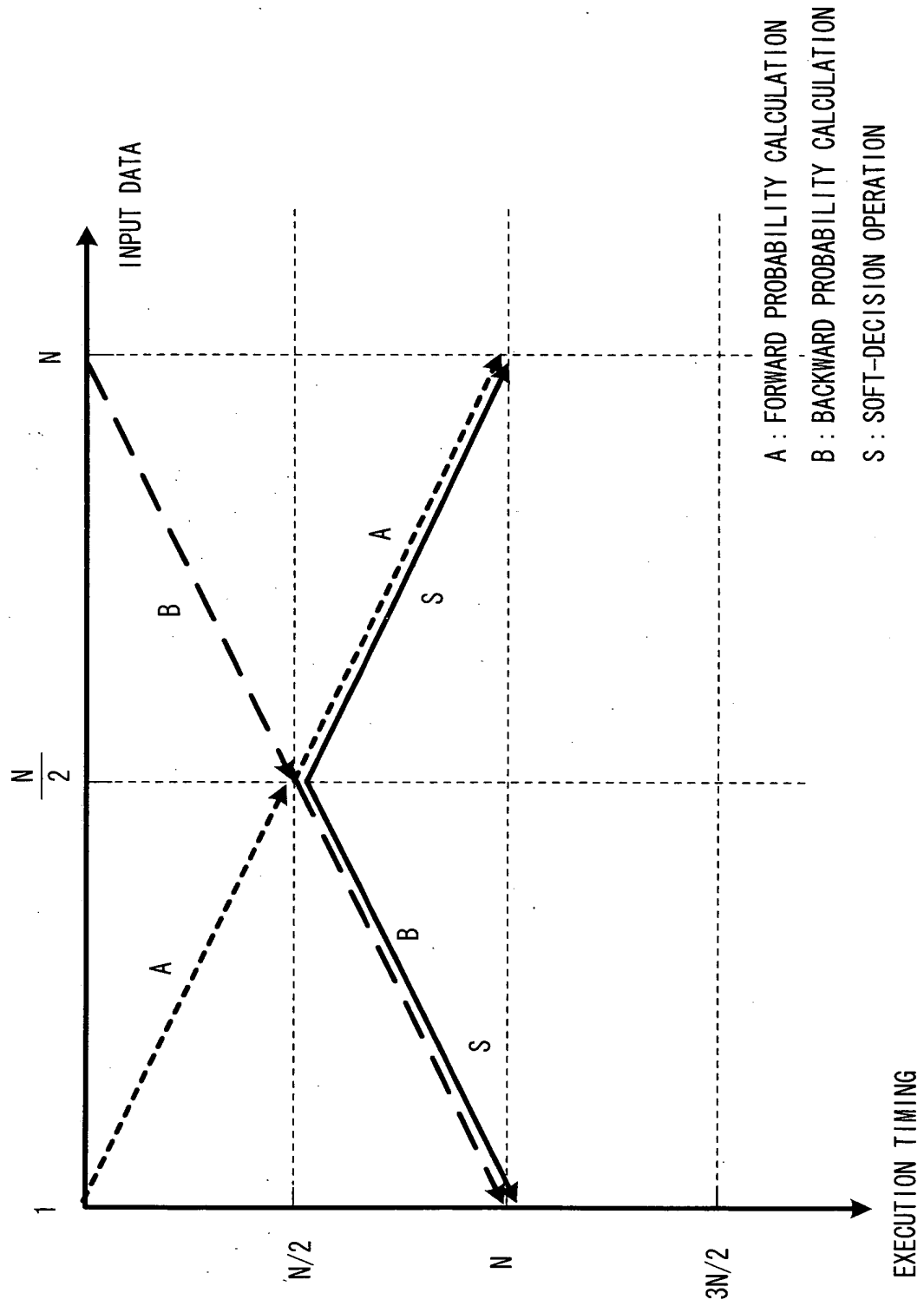


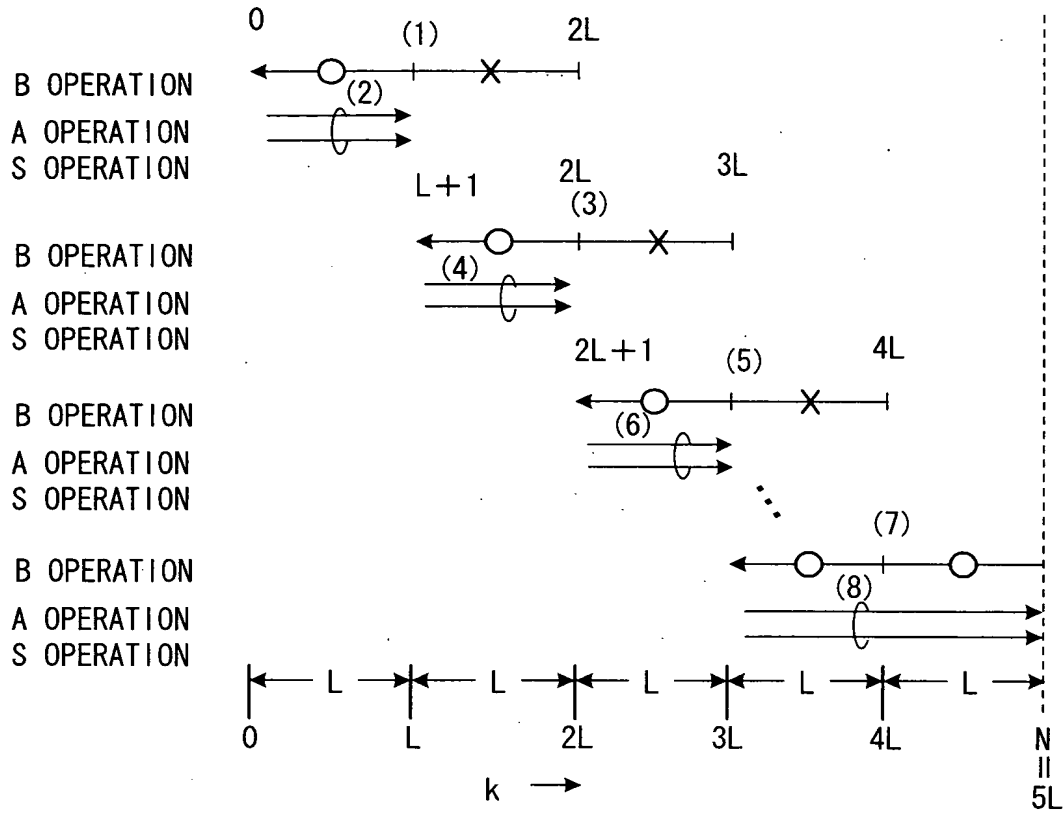
FIG. 18 PRIOR ART

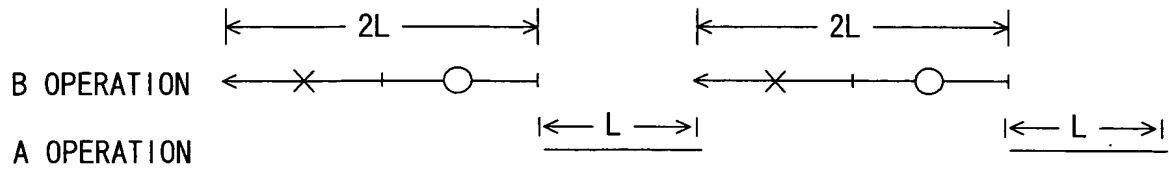
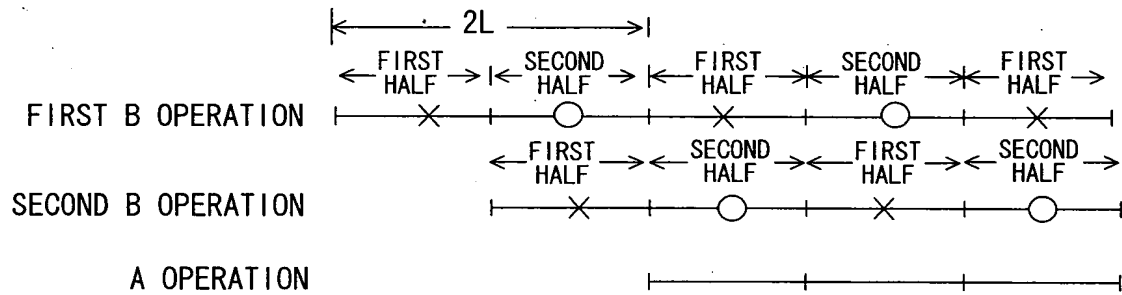
FIG. 19A PRIOR ART**FIG. 19B PRIOR ART**

FIG. 20 PRIOR ART

